## REMARKS/ARGUMENTS

This Amendment is being filed in response to the Office Action of June 15, 2010. Reconsideration and allowance of the application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1 and 3-5 are pending in the Application. Claims 1 and 4 are independent claims.

In the Office Action, claim 4 is objected to as being in improper form. In response, elements of the claim are rewritten to include action verbs and generally to be in a more suitable U.S. form. It is respectfully submitted that claim 4 is in proper form. Accordingly, withdrawal of the objection to claim 4 is respectfully requested.

Claims 1 and 3-5 are rejected under 35 U.S.C. §112, first paragraph as failing to comply with written description requirement. Independent claims 1 and 4 are amended to address the concerns raised in the Office Action and in accordance with the description of the specification at page 11, lines 10-12. Thus, it is respectfully submitted that the rejected claims are in proper form and withdrawal of the rejection is respectfully requested.

Claims 1 and 3-5 are rejected under 35 U.S.C. §112, second paragraph as being indefinite. With regard to the phrase "during the execution of the instruction", all claim elements/acts are performed during the executed VLSI instruction. The phrases related to "latency" are amended to render them "definite". The antecedent bases of the limitation "input data" were also corrected. Thus, it is respectfully submitted that the rejected claims are in proper form and withdrawal of the rejection is respectfully requested.

Claims 1 and 3-5 are rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,909,565 to Morikawa et al. ("Morikawa"). This rejection is respectfully traversed. It is respectfully submitted that claims 1 and 3-5 are allowable over the presented prior art reference for at least the following reasons.

Morikawa, as stated in its Abstract, describes a system having a main processor and a coprocessor for processing data according to instructions stored in memory. The system includes instruction detecting means for detecting coprocessor calculation instructions out of the instructions received from memory and coprocessor instruction detecting means for detecting coprocessor calculation instructions out of all of the instructions received from the memory. In other words, the processor and coprocessor in Morikawa execute (different) instructions that are designated, and later identified by the detecting means to be processed by that processor.

Claim 1 sets out "first and second functional units for performing one or more operations of an instruction at the same time". Only one instruction is executed in the recitation of claim 1. The executed instruction is of the Very Long Instruction Word type and the device of claim 1 and method of claim 4 shorten the amount of registers and the number of cycles required for execution of the VLIW instructions. Morikawa describes separate execution of dedicated instructions by two processors, this has little or nothing to do with simultaneous processing of a single VLIW instruction as recited in claim 1.

It is respectfully submitted that the apparatus of claim 1 is not anticipated or made obvious by the teachings of Morikawa. For example, Morikawa does not teach, disclose or suggest, amongst other patentable elements, (illustrative emphasis added) "first and

second functional units for performing one or more operations of an instruction at the same time, the first functional unit including a slave controller, the one or more operations having a different latency; and a master controller for controlling a schedule for executing the one or more operations by the first functional unit including input/output operations that are performed by the slave controller of the first functional unit, wherein said master controller synchronizes the first functional unit to use output data processed by the second functional unit during the execution of said instruction and to provide input data to the second functional unit during the execution of said instruction", as recited in claim 1, and as similarly recited in claim 4. In Morikawa, the processor and coprocessor execute different instructions that are designated by the detecting means to be processed by a given processor or coprocessor and as such, have little if anything to do with the pending claims.

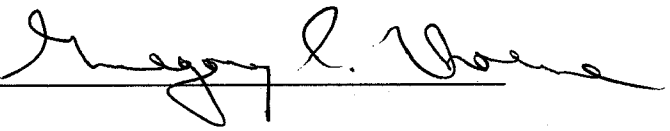
Based on the foregoing, the Applicant respectfully submits that independent claims 1 and 4 are patentable and notice to this effect is earnestly solicited. Claims 3 and 5 respectively depend from one of claims 1 and 4 and accordingly are allowable for at least this reason as well as for the separately patentable elements contained in each of the claims. Accordingly, separate consideration of each of the dependent claims is respectfully requested.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support

of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

Applicants have made a diligent and sincere effort to place this application in condition for immediate allowance and notice to this effect is earnestly solicited.

Respectfully submitted,

By 

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